IN THE CLAIMS

For the Examiner's convenience, a list of all claims is included below.

1. (Previously Presented) A method, comprising:

asserting an edge-triggered interrupt signal from an input/output interrupt controller located within a system logic device to a local interrupt controller located within a processor; and

delivering an interrupt pending signal from the processor to a power management unit located within the system logic device.

2. (Currently Amended) The method of claim 1, further comprising the ~~power management~~ system logic device causing the processor to enter a high power state if the processor is in a low power state when the processor delivers the interrupt pending signal to the power management unit.

3. (Previously Presented) The method of claim 2, wherein delivering an interrupt pending signal includes delivering the interrupt pending signal from the processor to the power management unit over a single signal line coupled between a single processor pin and the system logic device.

4. (Previously Presented) The method of claim 3, wherein causing the processor to enter a high power state includes the power management unit deasserting a stop clock signal.

5. (Previously Presented) A method, comprising:

asserting an edge-triggered interrupt signal from an input/output interrupt controller located within a system logic device to a local interrupt controller located within a processor;

setting a bit within the processor indicating that an interrupt is pending; and

polling the processor to determine if an interrupt is pending.

6. (Original) The method of claim 5, wherein polling the processor to determine if an interrupt is pending includes polling the processor to determine if an interrupt is pending only if the processor is in a low power state.

7. (Original) The method of claim 6, further comprising causing the processor to enter a high power state if the polling of the processor reveals that an interrupt is pending.

8. (Previously Presented) The method of claim 7, wherein causing the processor to enter a high power state includes deasserting a stop clock signal delivered from a power management unit located within the system logic device to the processor.

9. (Previously Presented) A system, comprising:

a processor including a local interrupt controller and an interrupt pending signal output;

a system logic device including an input/output interrupt controller coupled to the processor, the input/output interrupt controller to deliver an edge-triggered interrupt signal to the processor; and

a power management unit located within the system logic device including an interrupt pending signal input coupled to the interrupt pending signal output of the processor, the processor to assert the interrupt pending signal in response to the delivery of the edge-triggered interrupt signal.

10. (Previously Presented) The system of claim 9, wherein the processor further includes a stop clock signal input, the processor to cease executing instructions in response to an assertion of the stop clock signal by the power management unit.

11. (Currently Amended) The system of claim 10, wherein the power management unit ~~to~~ causes the processor to enter a high power state if the processor is in a low power state when the processor asserts the interrupt pending signal.

12. (Currently Amended) The system of claim 11, wherein the power management unit causes the processor to enter the high power state by ~~be~~ deasserting the stop clock signal.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)